

App. Ser. No. 10/600,779
Amendment dated October 25, 2004
Reply to Office action of September 28, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

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1. (Currently Amended) An analog to digital converter ("ADC"), comprising:

a band gap reference (BGR) circuit whose output is a direct analog input internally coupled to an analog input of the ADC;

a positive analog supply voltage (AVDD);

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a positive analog reference voltage (REFP); and

a voltage supply operationally coupled to both the positive analog supply voltage (AVDD) and the positive analog reference voltage (REFP);

wherein a measured BGR value is used by a CPU as a calibration constant for determining an AVDD value.

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2. (Cancelled)

3. (Currently Amended) The ADC of Claim 1, ~~wherein the ADC can measure the AVDD without using a divider~~ wherein the measured BGR value is used by the CPU as a calibration constant for determining a REFP value, and a Bit Weight value.

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4. (Currently Amended) The ADC of Claim 1, wherein the measured BGR value is inversely proportional to the actual AVDD value.

5. (Currently Amended) A system using a CPU, comprising:

an analog to digital converter ("ADC"), wherein the ADC includes:

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a band gap reference (BGR) circuit whose output is a direct analog input inter-
nally coupled to an analog input to the ADC;

a positive analog supply voltage (AVDD);

a positive analog reference voltage (REFP); and

5 a voltage supply operationally coupled to both the positive analog supply voltage
(AVDD) and the positive analog reference voltage (REFP);

wherein a measured BGR value is used by the CPU as a calibration constant for
determining an AVDD value.

6. (Cancelled)

10 7. (Currently Amended) The system of Claim 5, ~~wherein the ADC can measure the AVDD~~
~~without using a divider~~ wherein the measured BGR value is used by the CPU as a calibration
constant for determining a REFP value, and a Bit Weight value.

8. (Currently Amended) The system of Claim 5, wherein the measured BGR value is inversely
proportional to the actual AVDD value.

15 9. (Currently Amended) An application specific integrated circuit ("ASIC"), comprising:

an analog to digital converter ("ADC"), comprising:

a band gap reference (BGR) circuit whose output is a direct analog input inter-
nally coupled to an analog input of to the ADC;

a positive analog supply voltage (AVDD);

20 a positive analog reference voltage (REFP); and

a voltage supply operationally coupled to both the positive analog supply voltage
(AVDD) and the positive analog reference voltage (REFP);

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wherein a measured BGR value is used by a CPU as a calibration constant for determining an AVDD value.

10. (Cancelled)

11. (Currently Amended) The ASIC of Claim 9, ~~wherein the ADC can measure the AVDD~~
5 ~~without using a divider~~ wherein the measured BGR value is used by the CPU as a calibration
constant for determining a REFP value, and a Bit Weight value.

12. (Currently Amended) The system of Claim 9, wherein the measured BGR value is inversely proportional to the actual AVDD value.

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